LAB ASSIGNMENT No 9:

To Study the Types of FETs & Recognize the Operation Of MOSFETs Calculate Trans Conductance & Threshold Voltage

APPARATUS:

Power Electronics Board

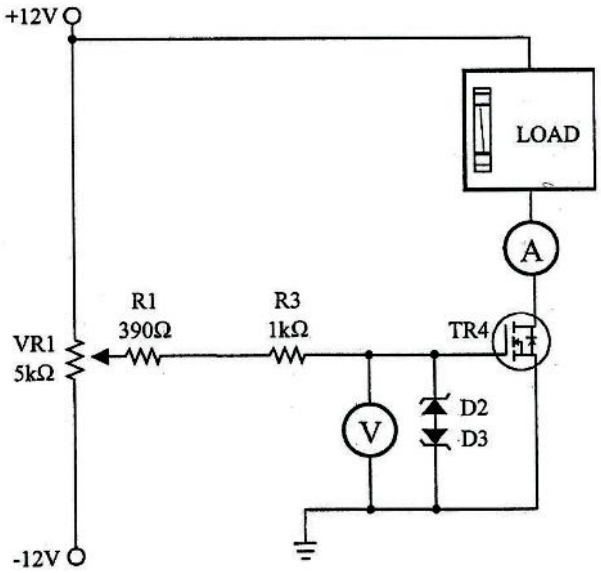
Oscilloscope

Multi meters

Connecting wires

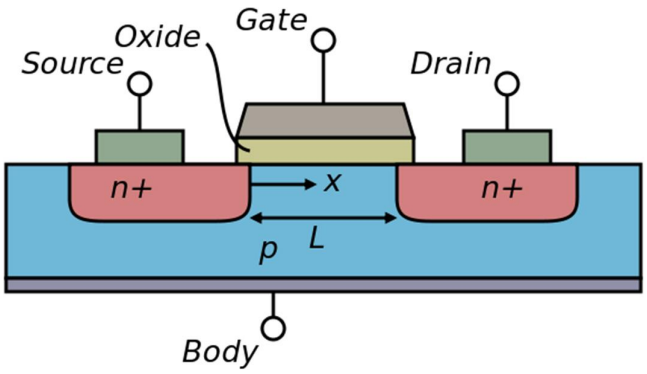
Signal Generator

DIAGRAM:



THEORY:

The field-effect transistor (FET) is a transistor that uses an electric field to control the shape and hence the conductivity of a channel of one type of charge carrier in a semiconductor material. FETs are unipolar transistors as they involve single-carrier-type operation.



FETs can be majority-charge-carrier devices, in which the current is carried predominantly by majority carriers, or minority-charge-carrier devices, in which the current is mainly due to a flow of minority carriers. The device consists of an active channel through which charge carriers, electrons or holes, flow from the source to the drain.

The channel of a FET is doped to produce either an n-type semiconductor or a p-type semiconductor. The drain and source may be doped of opposite type to the channel, in the case of depletion mode FETs, or doped of similar type to the channel as in enhancement mode FETs. Field-effect transistors are also distinguished by the method of insulation between channel and gate.

Types of FETs include:

JFET MOSFET

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals.

Cutoff mode:

When $V_{GS} < V_{th}$:

Where V_{GS} is gate-to-source bias and V_{th} is the threshold voltage of the device. According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source.

While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current.

Linear region:

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$:

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages.

Saturation mode:

When $V_{GS} > V_{th}$ and $V_{DS} \geq (V_{GS} - V_{th})$:

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the source voltage, the electrons spread out, and conduction is not through a narrow channel.

The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage

The minimum value of Gate voltage required to form a channel and allow current to flow is called the Threshold Voltage V_T. The degree of control exercised by the Gate voltage over the Drain current is a measure of the sensitivity of the device.

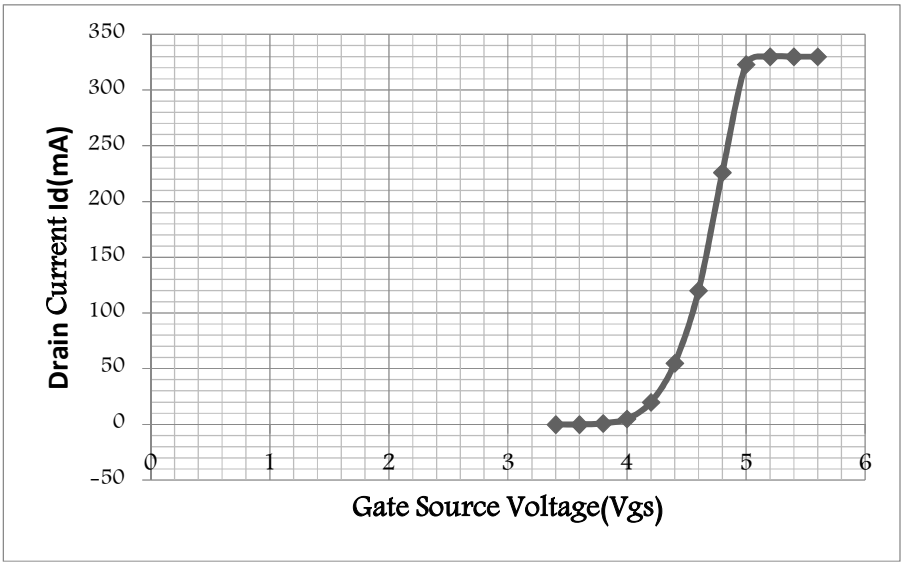
The parameter Trans-conductance (Mutual Conductance) (gm, yf_s) is defined as= $\frac{\delta I_D}{\delta V_{GS}}$

The unit of Trans-conductance is siemens & If the values of Drain Current are taken in mA then the result will be in milisiemens mS Conductance is the reciprocal of Resistance and is measured in Siemens.

TABLE:

Input Voltage (V)	Output Current (mA)	Input Voltage (V)	Output Current (mA)
3.1	0	4.4	115
3.4	0	4.6	220
3.6	1	4.8	319
3.9	6	5.2	333
4.1	17	5.5	335
4.2	50	5.6	335

GRAPH:



LAB ASSIGNMENT No 10:

Calculate and compare the input resistance of BJT & the MOSFET

APPARATUS:

Power Electronics Board

Oscilloscope

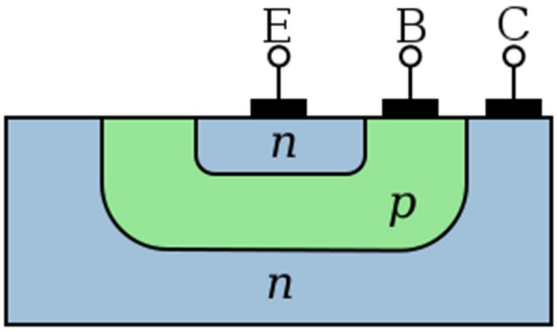
Multi meters

Connecting wires

Signal Generator

THEORY:

BJT consists of three differently doped semiconductor regions, the emitter region, the base region and the collector region. These regions are, respectively, p type, n type and p type in a PNP transistor, and n type, p type and n type in an NPN transistor. Each semiconductor region is connected to a terminal, appropriately labeled: emitter (E), base (B) and collector (C).



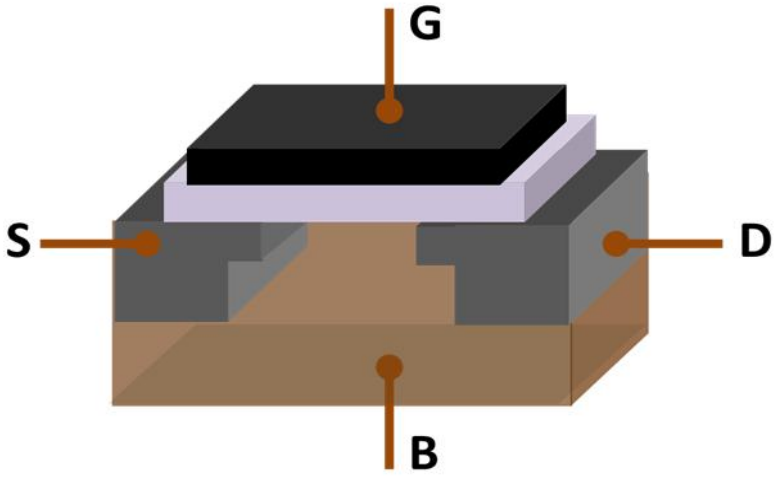
The base is physically located between the emitter and the collector and is made from lightly doped, high resistivity material. The collector surrounds the emitter region, making it almost impossible for the electrons injected into the base region to escape without being collected, thus making the resulting value of α very close to unity, and so, giving the transistor a large β.

A cross section view of a BJT indicates that the collector–base junction has a much larger area than the emitter–base junction.

The bipolar junction transistor, unlike other transistors, is usually not a symmetrical device. This means that interchanging the collector and the emitter makes the transistor leave the forward active mode and start to operate in reverse mode.

Small changes in the voltage applied across the base–emitter terminals causes the current that flows between the emitter and the collector to change significantly. This effect can be used to amplify the input voltage or current. BJTs can be thought of as voltage-controlled current sources, but are more simply characterized as current-controlled current sources, or current amplifiers, due to the low impedance at the base.

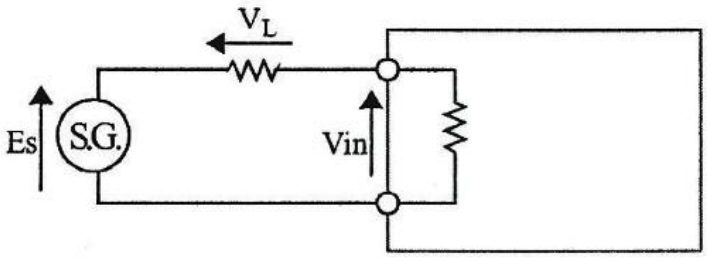
Metal Oxide Semiconductor Field-Effect Transistor, or simply MOSFET, and sometimes MOS transistor, is a voltage-controlled device. Unlike the BJT, there is no base current present. However, there's a field produced by a voltage on the gate. This allows a flow of current between the source and the drain. This current flow may be pinched-off, or opened, by the voltage on the gate.



In this transistor, a voltage on an oxide-insulated gate electrode can generate a channel for conduction between the other contacts the source and drain. MOSFETs handle power more efficiently. MOSFETs, nowadays, are the most common transistor used in digital and analog circuits, replacing the then very popular BJTs.

The FET is a voltage driven device, the output current being controlled by the input voltage. The insulation between the Gate and the channel prevents any input current flowing. The input impedance is very high.

The BJT is a current driven device. The output current is controlled by the input current and its input impedance can be very low.

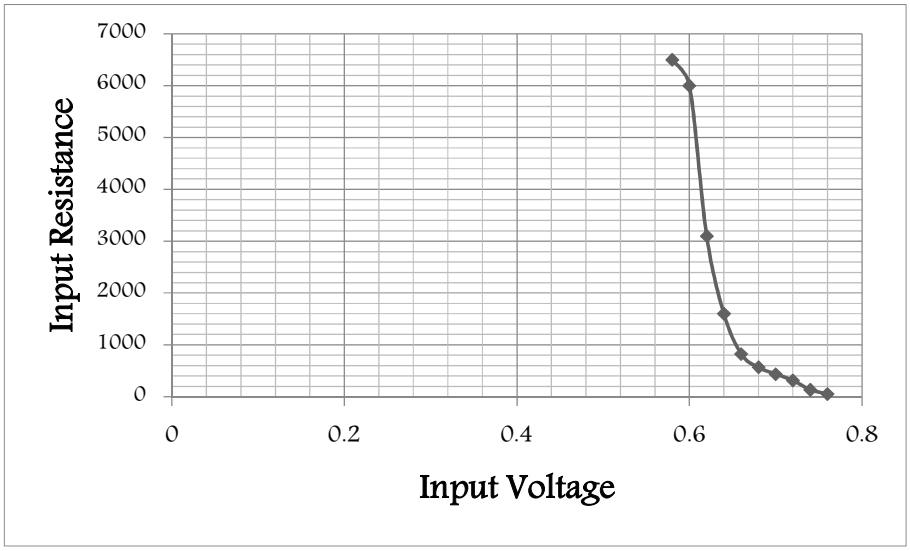


Low input impedance can be a serious disadvantage when feeding the stage from a medium-to-high impedance source. A large proportion of the source voltage (E_s) may be lost across its own output impedance (V_L), leaving a much smaller value of input voltage (V_{in}) at the input terminals.

TABLE:

Input Voltage	Input Current	Input Resistance	Input Voltage	Input Current	Input Resistance
0.50	0	-	0.65	1.2	561 Ω
0.59	0.1	5.8K Ω	0.68	1.5	427 Ω
0.62	0.2	3K Ω	0.71	2.1	298 Ω
0.65	0.4	1.4K Ω	0.74	5.3	126 Ω
0.67	0.8	815 Ω	0.77	13.4	51 Ω

GRAPH:



LAB ASSIGNMENT No 11:

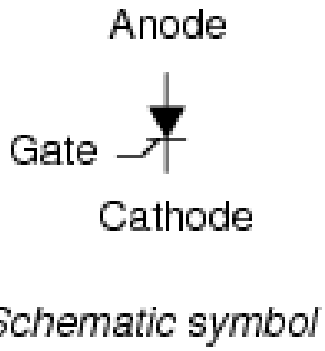
To Measure The Gate Firing Voltage & Anode-Cathode Voltage Of Thyristor

APPARATUS:

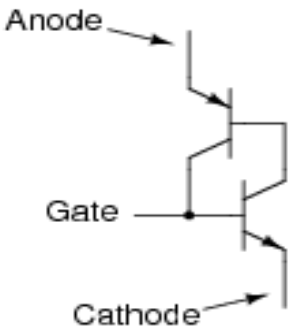
Power supply
Connecting wires
Trainer
Multimedia
Oscilloscope

THEORY:

A thyristor is a two- to four-lead solid-state semiconductor device with four layers of alternating N and P-type material. They act exclusively as bistable switches, conducting when their gate receives a current trigger, and continue to conduct while they are forward biased that is, while the voltage across the device is not reversed.



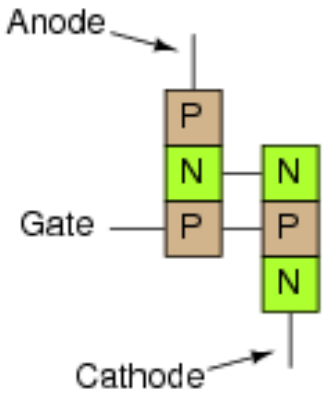
Schematic symbol



Equivalent schematic

A three-lead thyristor is designed to control the larger current of its two leads by combining that current with the smaller current or voltage of its other lead known as its control lead.

On the other hand, a two-lead thyristor is designed to 'switch on' if the potential difference between its leads is sufficiently large – a value representing its breakdown voltage.



Physical diagram

The thyristor is a four-layered, three terminal semiconductor device, with each layer consisting of alternately N-type or P-type material, for example P-N-P-N. The name thyristor is derived from combination of THYR(Thyratron tubes) + istor(resistor).The main terminals, labelled anode and cathode, are across all four layers. The control terminal, called the gate, is attached to p-type material near the cathode.

The operation of a thyristor can be understood in terms of a pair of tightly coupled bipolar junction transistors, arranged to cause a self-latching action.

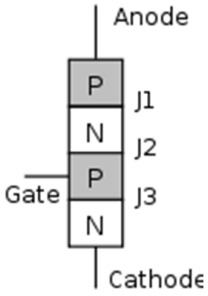
Thyristors have three states:

Reverse blocking mode: Voltage is applied in the direction that would be blocked by a diode.

Forward blocking mode: Voltage is applied in the direction that would cause a diode to conduct, but the thyristor has not been triggered into conduction.

Forward conducting mode: The thyristor has been triggered into conduction and will remain conducting until the forward current drops below a threshold value known as the "holding current"

The thyristor has three p-n junctions serially named J_1, J_2, J_3 from the anode.



Layer diagram of thyristor

When the anode is at a positive potential V_{AK} with respect to the cathode with no voltage applied at the gate, junctions J_1 and J_3 are forward biased, while junction J_2 is reverse biased. As J_2 is reverse biased, no conduction takes place.

Now if V_{AK} is increased beyond the breakdown voltage V_{BO} of the thyristor, avalanche breakdown of J_2 takes place and the thyristor starts conducting.

If a positive potential V_G is applied at the gate terminal with respect to the cathode, the breakdown of the junction J_2 occurs at a lower value of V_{AK}. By selecting an appropriate value of V_G, the thyristor can be switched into the on state quickly.

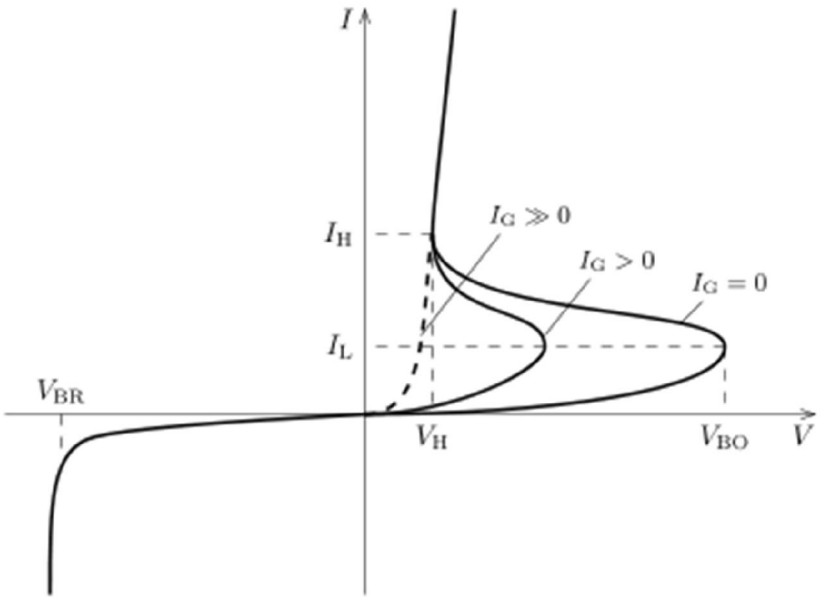
Once avalanche breakdown has occurred, the thyristor continues to conduct, irrespective of the gate voltage, until the potential V_{AK} is removed or the current through the device (anode–cathode) is less than the holding current specified by the manufacturer.

The gate pulses are characterized in terms of gate trigger voltage (V_{GT}) and gate trigger current (I_{GT}). Gate trigger current varies inversely with gate pulse width in such a way that it is evident that there is a minimum gate charge required to trigger the thyristor.

In a conventional thyristor, once it has been switched on by the gate terminal, the device remains latched in the on-state i.e. does not need a continuous supply of gate current to remain in the on state, providing the anode current has exceeded the latching current (I_L). As long as the anode remains positively biased, it cannot be switched off until the anode current falls below the holding current (I_H).

A thyristor can be switched off if the external circuit causes the anode to become negatively biased a method known as natural, or line, commutation. In some applications this is done by switching a second thyristor to discharge a capacitor into the cathode of the first thyristor. This method is called forced commutation.

After the current in a thyristor has extinguished, a finite time delay must elapse before the anode can again be positively biased and retain the thyristor in the off-state. This minimum delay is called the circuit commutated turn off time (t_Q). Attempting to positively bias the anode within this time causes the thyristor to be self-triggered by the remaining charge carriers (holes and electrons) that have not yet recombined.



LAB ASSIGNMENT No 13:

To study the Resistive-Capacitive firing Circuit (Half wave)

APPARATUS:

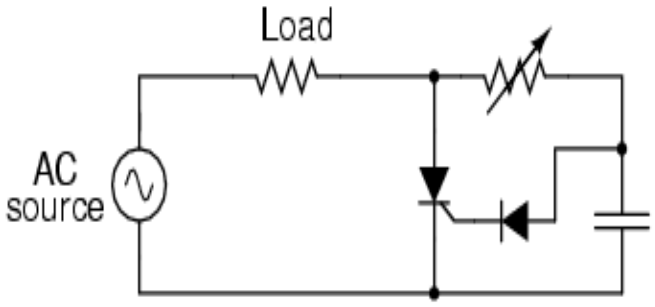
Power Electronics Board

Oscilloscope

Multi meters

Connecting wires

DIAGRAM:



THEORY:

A power control circuit has a thyristor bridge interposed between a.c. buses connected to an a.c. power supply and a load. The firing circuit for the thyristors of the bridge includes a light actuated controlled rectifier for generating firing pulses. Two series connected resistor-capacitor pairs are connected in series across the a.c. buses. Taps intermediate the resistors and capacitors provide an energizing anode voltage to the controlled rectifier reduced with respect to the a.c. voltage in the buses.

The triggering angle control limitation of the diode resistance triggering circuit can be overcome by the diode-resistance-capacitance triggering circuit. The figure shows the RC-half wave trigger circuit. The conduction period can

be controlled over the full 180° range. By varying the value of R1, the trigger can be controlled from 0 to Π.During the positive half cycle, the capacitor C charges to the trigger voltage of the thyristor in a time determined by the RC time constant and the applied anode voltage. During the negative half cycle, the capacitor charges to the peak supply voltage at $\omega t = (-\Pi/2)$.

After this period,the supply voltage decreases and reaches zero at $\omega t=0$. During this period the capacitor voltage becomes positive during the positive half cycle of the ac input, the capacitor begins to charge through the variable resistance R1, in the opposite direction and as soon as it charges to a positive voltage equal to the gate trigger voltage, the thyristor turns ON. Here the diode D1 is used to prevent the negative voltage between the gate and the cathode through the diode D2 during the negative half-cycle.

At Large Resistance:

When the resistor 'R' is large, the time taken for the capacitance to charge from -Vm to –Vgt is large, resulting in larger firing angle and lower load voltage.

At Small Resistance:

When 'R' is set to a smaller value, the capacitor charges at a faster rate towards Vgt resulting in early triggering of SCR and hence VL is more. When the SCR triggers, the voltage drop across it falls to 1 – 1.5V. This in turn lowers, the voltage across R & C. Low voltage across the SCR during conduction period keeps the capacitor discharge during the positive half cycle.

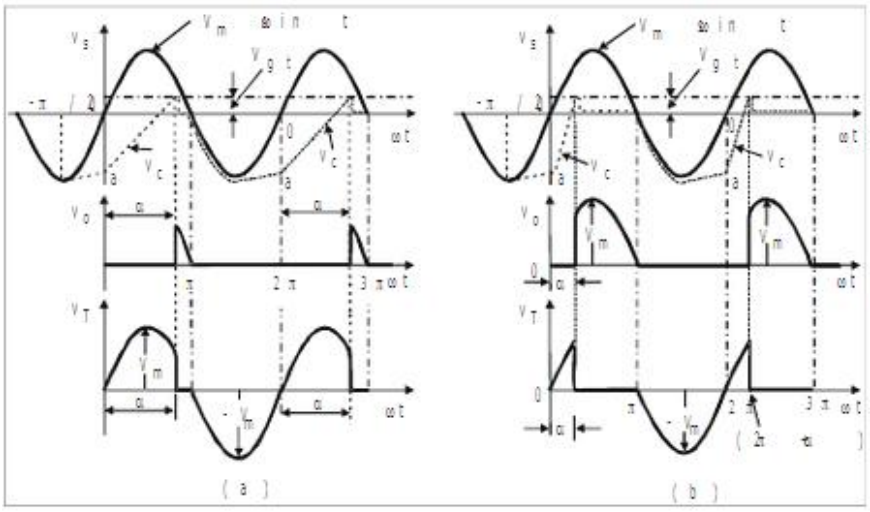


Fig.: Waveforms for RC half-wave trigger circuit

(a) High value of R **(b) Low value of R**

LAB ASSIGNMENT No 14:

To study the Resistive-Capacitive firing Circuit (Full wave)

APPARATUS:

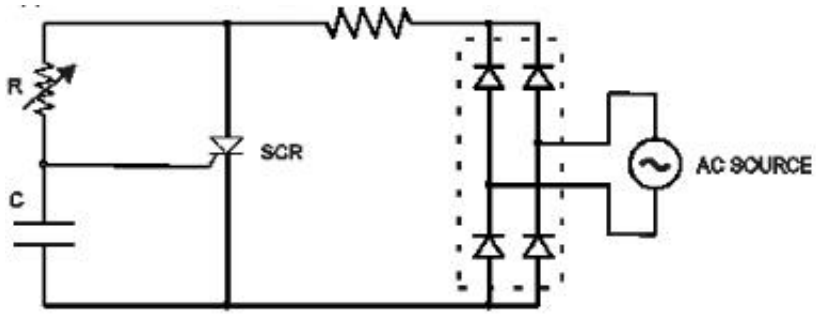
Power Electronics Board

Oscilloscope

Multi meters

Connecting wires

DIAGRAM:



RC Triggering (Full Wave)

THEORY:

A power control circuit has a thyristor bridge interposed between a.c. buses connected to an a.c. power supply and a load. The firing circuit for the thyristors of the bridge includes a light actuated controlled rectifier for generating firing pulses. Two series connected resistor-capacitor pairs are connected in series across the a.c. buses. Taps intermediate the resistors and capacitors provide an energizing anode voltage to the controlled rectifier reduced with respect to the a.c. voltage in the buses.

The triggering angle control limitation of the diode resistance triggering circuit can be overcome by the diode-resistance-capacitance triggering circuit. The figure shows the RC-full wave trigger circuit.

In the RC-half wave trigger circuit power can be delivered to the load only during the positive half cycle of AC because the SCR conducts only when it is forward biased. This limitation can be overcome in several ways; here the ac line voltage is converted to pulsating dc by the full-wave diode bridge. This allows the SCR to be triggered ON for both half cycle of the line voltage, which doubles the available power to the load. The initial voltage, V by which the capacitor C charges is almost zero. Capacitor C is set to this low positive voltage by the clamping action of the SCR gate. When the capacitor charges to a voltage equal to Vgt, SCR triggers and rectified voltage Edc appears across load as E_L.

At Large Resistance:

When the resistor 'R' is large, the time taken for the capacitance to charge from -Vm to –Vgt is large, resulting in larger firing angle and lower load voltage.

At Small Resistance:

When 'R' is set to a smaller value, the capacitor charges at a faster rate towards Vgt resulting in early triggering of SCR and hence VL is more. When the SCR triggers, the voltage drop across it falls to 1 – 1.5V. This in turn lowers, the voltage across R & C. Low voltage across the SCR during conduction period keeps the capacitor discharge during the positive half cycle.

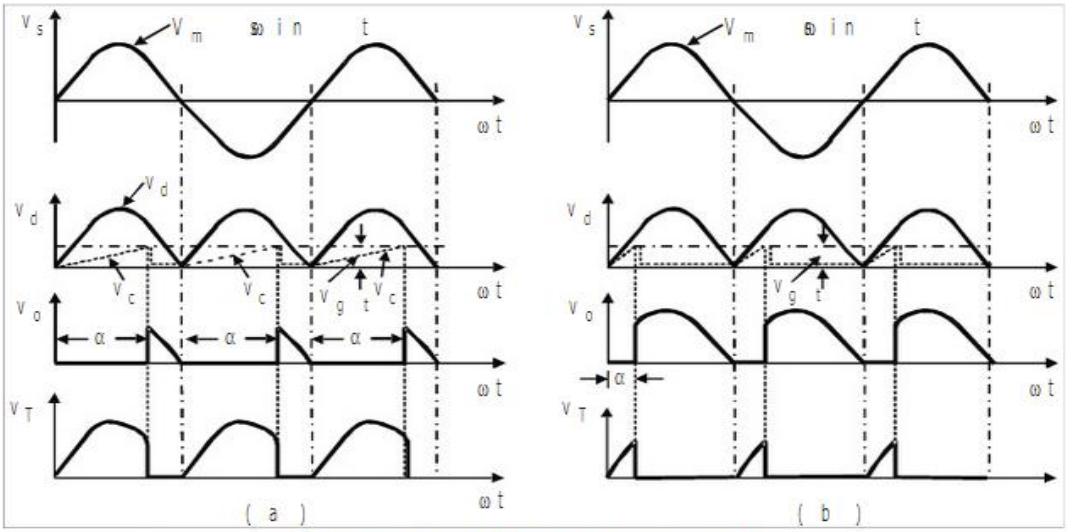


Fig: Wave-forms for RC full-wave trigger circuit

(a) High value of R **(b) Low value of R**

LAB ASSIGNMENT No 15:

To Study The Triggering Of SCR Using UJT

APPARATUS:

Power supply

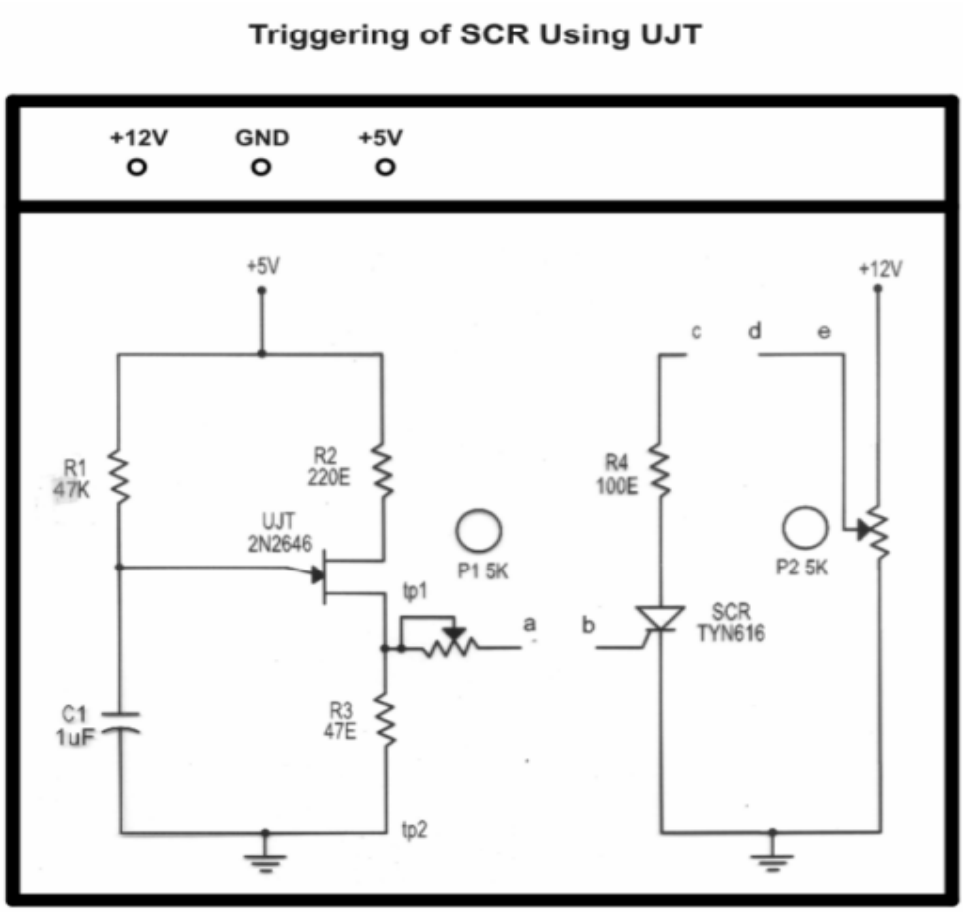
Connecting wires

Trainer

Multimedia

Oscilloscope

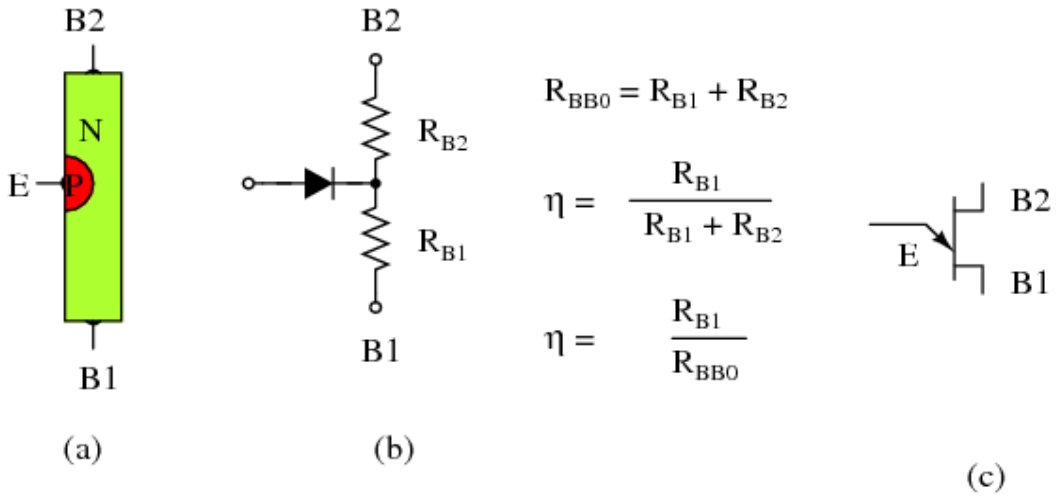
DIAGRAM:



THEORY:

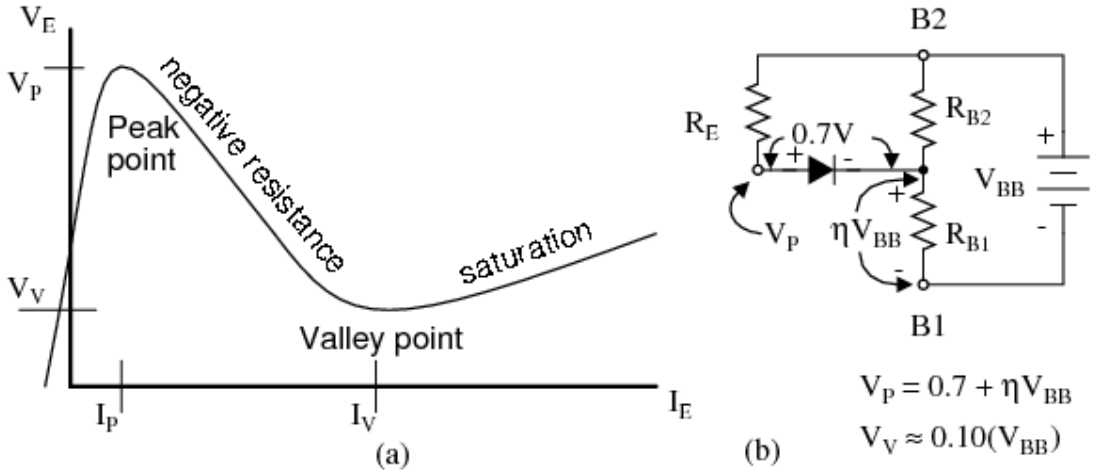
Unijunction transistor:

Although a unijunction transistor is not a thyristor, this device can trigger larger thyristors with a pulse at base B1. A unijunction transistor is composed of a bar of N-type silicon having a P-type connection in the middle. The connections at the ends of the bar are known as bases B1 and B2. The P-type mid-point is the emitter. With the emitter disconnected, the total resistance R_{BBO} is the sum of R_{B1} and R_{B2}. R_{BBO} ranges from 4-12 kΩ for different device types. The intrinsic standoff ratio η is the ratio of R_{B1} to R_{BBO}. It varies from 0.4 to 0.8 for different devices.



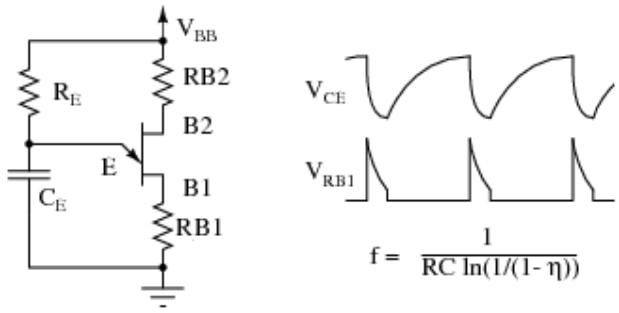
Unijunction transistor: (a) Construction, (b) Model, (c) Symbol

The Unijunction emitter current vs voltage characteristic curve shows that as V_E increases, current I_E increases up I_P at the peak point. Beyond the peak point, current increases as voltage decreases in the negative resistance region. The voltage reaches a minimum at the valley point. The resistance of R_{B1}, the saturation resistance is lowest at the valley point.



Unijunction transistor: (a) emitter characteristic curve, (b) model for V_P.

The relaxation oscillator is an application of the unijunction oscillator. R_E charges C_E until the peak point. The unijunction emitter terminal has no effect on the capacitor until this point is reached. Once the capacitor voltage, V_E, reaches the peak voltage point V_P, the lowered emitter-base1 E-B1 resistance quickly discharges the capacitor. Once the capacitor discharges below the valley point V_V, the E-RB1 resistance reverts back to high resistance, and the capacitor is free to charge again.



Unijunction transistor relaxation oscillator and waveforms.

During capacitor discharge through the E-B1 saturation resistance, a pulse may be seen on the external B1 and B2 load resistors. The load resistor at B1 needs to be low to not affect the discharge time. The external resistor at B2 is optional. It may be replaced by a short circuit. The approximate frequency is given by $1/f = T = RC$. A more accurate expression for frequency.

The charging resistor R_E must fall within certain limits. It must be small enough to allow I_P to flow based on the V_{BB} supply less V_P. It must be large enough to supply I_V based on the V_{BB} supply less V_V.

$$R_E < \quad V_{BB} - V_p / I_P$$

At the valley point, V_v

$$I_E = I_V \text{ and } V_E = V_V \text{ so that}$$
$$V_E = V_{BB} - I_{RE} R_E$$

So

$$R_{E(MIN)} = V_{BB} - V_E / I_{RE} = V_{BB} - V_V / I_V$$
$$R_E > = V_{BB} - V_V / I_V$$

So, the range of resistor R_E is given as:

$$V_{BB} - V_P / I_P > R_E > V_{BB} - V_V / I_V$$

The resistor R is chosen small enough so as to ensure that SCR is not turned on by voltage V_R when emitter terminal E is open or $I_E = 0$

The voltage $V_R = V_{BB} R/(R + R_{BB})$ for open-emitter terminal.

The capacitor C determines the time interval between triggering pulses and the time duration of each pulse. By varying R_E, we can change the time constant $R_E C$ and alter the point at which the UJT fires. This allows us to control the conduction angle of the SCR, which means the control of load current.

TABLE:

Sr No.	I_G (mA)	V_{AC} (V)	I_{AC} (mA)
1.	0.00	2	2.4
2.	0.05	3.46	2.58
3.	0.07	4.31	2.61
4.	0.08	5.12	2.65
5.	0.11	6.81	2.67
6.	0.12	8.6	2.73
7.	0.14	10	2.77
8.	0.15	12	2.85

CONCLUSIONS:

UJT is a triggering circuit for SCR. Unless resistance firing circuit and RC firing circuit it dissipate much less power.

Its efficiency is better than resistance firing circuit and RC firing circuit. It has negative resistance characteristics. When voltage reaches to a certain limit UJT triggers, voltage goes down and current increases.

LAB ASSIGNMENT No 16:

To Study The Triggering Of SCR Using IC 555

APPARATUS:

Power supply

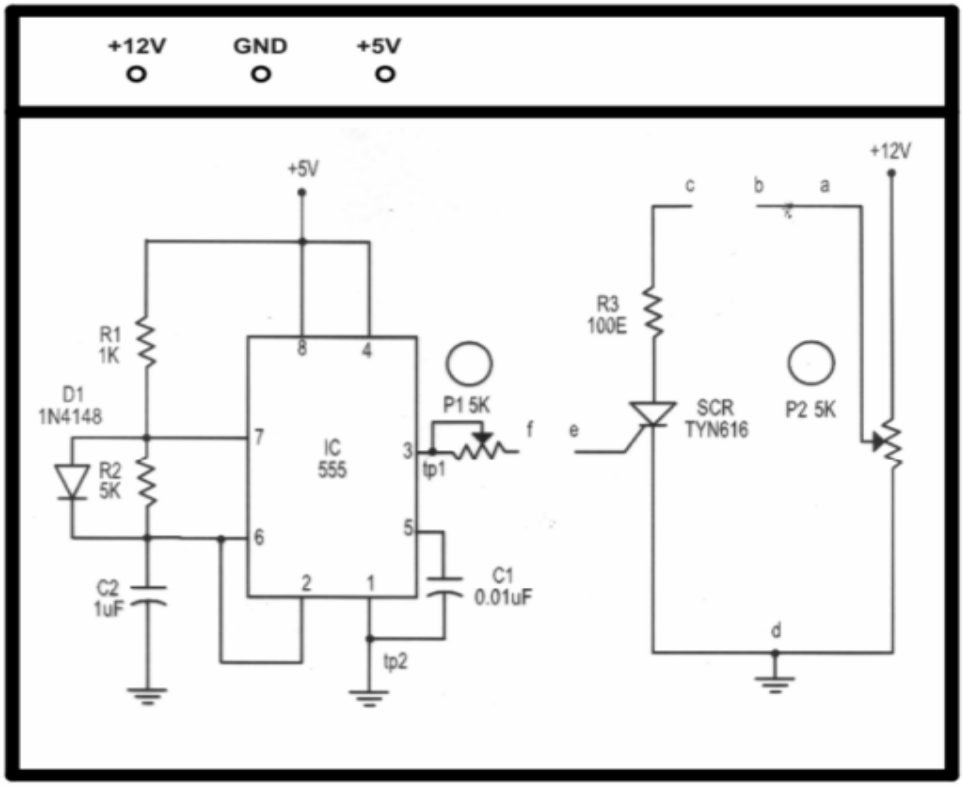
Connecting wires

Trainer

Multimedia

Oscilloscope

DIAGRAM:



THEORY:

Triggering of SCR using IC 555 :

The Astable and Monostable circuits are so commonly required the special monolithic IC called IC timers, have been made available. The 555 IC, which has gained wide acceptance in terms of cost and versatility. Some typical applications are Monostable and Astable Multivibrators, dc-dc converters, digital logic probes, waveform generators, Analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, etc.

The device 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillations. The 555 IC used for triggering of SCR in both dc and ac circuits. An Astable timer operation is achieved by adding resistor RB. In the Astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a Multivibrator. When the timer output is high, its internal discharging Tr. turns off and the VC1 increases by exponential function with the time constant (RA+RB)*C.

When the VC1, or the threshold voltage, reaches 2Vcc/3, the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This in turn turns on the discharging Tr. and the C1 discharges through the discharging channel formed by RB and the discharging Tr. When the VC1 falls below Vcc/3, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging Tr. turns off and theVC1 rises again.

In the above process, the section where the timer output is high is the time it takes for the VC1 to rise from Vcc/3 to 2Vcc/3, and the section where the timer output is low is the time it takes for the VC1 to drop from 2Vcc/3 to Vcc/3. Since

the duration of the timer output high state (tH) is the amount of time it takes for the VC1 (t) to reach 2Vcc/3,

Since the duration of the timer output low state (tL) is the amount of time it takes for the VC1(t) to reach Vcc/3,

Since RD is normally RB>>RD although related to the size of discharging Tr.,

tL = 0.693RBC1 (10)

Consequently, if the timer operates in Astable, the period is the same with 'T=tH + tL= 0.693(RA+RB) C1+ 0.693RBC1= 0.693(RA+2RB) C1' because the period is the sum of the charge time and discharge time. And since frequency is the reciprocal of the period, the following applies.

The output pulse from 555 is connected to the gate of scr. By using a pot the gate current can be controlled and monitor the anode to cathode current. It will show at which point the scr is getting triggered.

TABLE:

Sr No.	I_G (mA)	V_{AC} (V)	I_{AC} (mA)
1.	0.22	11.74	0
2.	1.73	11.67	11
3.	3.3	9.4	19
4.	4.5	9.05	21
5.	6.7	9.04	24
6.	8.3	8.94	23
7.	15.0	8.88	21
8.	19.2	8.86	20
9.	28.4	0.15	85